REMARKS

This is intended to be a complete response to the Official Action mailed March 8, 2006, in which claims 19-21 were rejected. Claims 19-20 have been amended herein and new claims 24-26 have been added.

REJECTION UNDER §103(a)

Claims 19-21 stand rejected under 35 U.S.C. 103(a) as being unpatentable over US 5,430,933 (Marx) in view of US 2001/0002163 A1 (Imasu).

In the rejection it is stated:

> "Marx discloses, referring primarily to figures 3-6, a shielded interconnect structure for interconnecting plural devices on a printed circuit board, the shielded interconnect structure comprising; plural first level conductive sites (18), disposed on an upper surface of the printed circuit board, each first level conductive site being adapted for electrical connection to one or more of the plural devices; plural second level conductive traces (12); disposed on a buried level of the printed circuit board; plural micro-vias (28) providing electrical connection from selected ones of the first level conductive sites to selected ones of the second level conductive traces; one or more third level conductive traces (12), disposed on a further buried level of the printed circuit board; a conductive shield comprising; a top shield layer (20) disposed on an upper surface of the printed circuit board, a conductive side wall (40), electrically connected to the top shield layer, and a bottom shield layer (70), electrically connected to the conductive side wall, buried within the printed circuit board at a level beneath the further buried level; wherein a trench is formed in the printed circuit board

> surrounding the first level conductive sites, the second level conductive traces, and the third level conductive traces, the conductive side wall being formed on a wall of the trench." (emphasis added)

Applicant respectfully traverses the rejection on the basis that neither Marx alone, nor Marx in view of Imasu teaches the claimed invention, as discussed in further detail below.

Claim 19 has been amended to delete limitations (related to microvia connections) which are not necessary to distinguish the claim over the art. The limitations deleted from claim 19 have been incorporated into new dependent claims 24-26.

Claim 19 has been further amended to indicate that the first, second and third conductive traces are a part of a signal line, and that the trenches are parallel at least in part to the signal lines, and that at least one trench is positioned between adjacent signal lines.

Regarding the basis for the rejection, attention is drawn to the statement therein that Marx teaches:

> "a trench is formed in the printed circuit board surrounding the first level conductive sites, the second level conductive traces, and the third level conductive traces, the conductive side wall being formed on a wall of the trench."

Marx in fact does not teach a trench in the completed PCB.

Marx teaches the presence of a trench 40 in the PCB only during an intermediate step in manufacture of the PCB, as indicated in Col. 9, lines 1-16

> "Predetermined locations on the process panel 72 are routed in the border region 74 to provide circuit board boundary apertures. These are in the form of a plurality of in-series slots 40 which extend through the sandwich arrangement. The slots 40 are located and orientated such that their inwardly disposed side surfaces 42 form parts of edges 50 of the final multiple layer printed circuit board 60. Formation of the slots 40 cuts through and exposes cut edges of all conductive layers 70a along the inwardly disposed side surface 42 of each slot 40. The side surfaces 42 are longer that the widths of the bridges 44. Predetermined spaces or bridges 44 between adjacent slots 40 are required so that the printed circuit board 60 may still be structurally supported by the process panel 72, during the remainder of the manufacturing process."

and, in Col. 9, lines 48-62:

> "Freeing the multiple layer printed circuit board 60 from the process panel 72 is achieved by simply severing across each bridge 44 on each of the four sides of the multiple layer printed circuit board 60 along a line which is colinear with the inward disposed surface 42 of a corresponding slot 40. The finished multiple layer printed circuit board 60 of FIG. 3 has edge surfaces 50 coated with conductive edge shielding layers 43 formed by the plating on inward disposed surfaces 42 of the sloes 40 and severed edge regions 52 produced across the bridges 44 and which are devoid of conductive material and hence expose a small portion of the sandwich arrangement; the conductive (electroplated) edge shielding layers 43 being integral with the top and bottom conductive layers 20, 22."

As can be seen from the description of Marx, Marx clearly teaches away from leaving trenches in the completed PCB. The trench (slot 40) used in Marx disappears when the PCB 60 is separated from the process panel 72 along the

grooves created by the slots 40.

Thus, the completed PCB of Marx does not have "trenches," contrary to examiner's assertion in the office action.

Moreover, as claimed herein at least one trench in the PCB is positioned between a pair of adjacent signal lines. This of course is not taught by Marx since the slots of Marx are positioned on the periphery of the device. Further, as Marx teaches the elimination of trenches, rather than their inclusion, there is no motivation in the art to modify the finished PCBs of Marx to include trenches.

In view of above, applicant respectfully requests reconsideration and withdrawal of the rejection under §103(a).

SECONDARY REFERENCES

The secondary reference U.S. 5,768,109 has been reviewed and determined not to teach the invention as claimed herein.

CONCLUSION

In view of the above, applicant submits the claims are now in a condition for reference and requests issuance of a Notice of Allowance.

Respectfully submitted,

Christopher W. Corbett, Ph.D.
Reg. No. 36,109
DUNLAP CODDING & ROGERS, P.C.
P.O. Box 16370
Oklahoma City, Oklahoma 73113
Telephone: 405/607-8600
Facsimile: 405/607-8686

Agent for Applicant